Apparatus and Method for Random Pattern Built In Self-test

Abstract

An apparatus permits built-in self-test ("BIST") of an IC that includes a memory element 104 having one or more impermissible operations. A code generator 401 accepts a clock signal 218 and generates a test code in response to it. A decoder 402 accepts the test code and generates at least two output lines 318, 319, 320, 321 where when in a decode enabled condition, the output lines 318, 319, 320, 321 are responsive to the test code and reflect a value that is combined with respective memory access lines comprising first and second write address outputs 309, 310 and first and second read address outputs 311, 312 as well as enable bits from first and second write enable registers 210, 211 and first and second read enable registers 214, 215 to disable the one or more impermissible operations. When the decoder 402 is in a decode disabled condition, the output lines 318, 319, 320, 321 reflect a value that when combined with the respective memory access lines enables all possible memory operations.